NGD4300-Q100

4 A peak high-performance dual MOSFET gate driver

Rev. 2.1 — 18 July 2025 Product data sheet

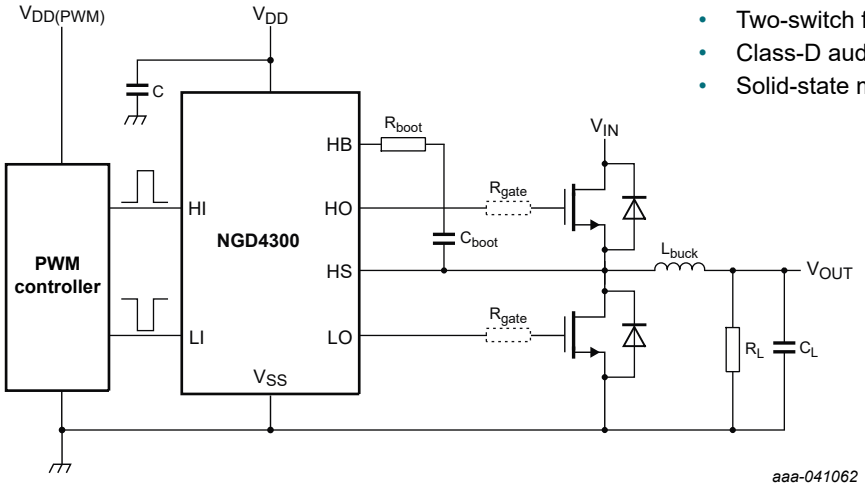
1. General description

The NGD4300-Q100 is a high-performance gate driver designed to drive both high-side and low-side N-channel MOSFETs in a synchronous buck or a half-bridge configuration. The floating high-side driver can work with rail voltages up to 120 V and uses a bootstrap supply with an integrated diode. Both low-side and high-side output drivers have an independent undervoltage lockout (UVLO) circuit which disables the output driver when the driver supply is below its threshold level. The NGD4300-Q100 accepts input control signals complying with both TTL and CMOS signaling as low as 2.5 V (±10%). The low voltage, provided by an internal voltage regulator, is used to supply circuitry in signal paths controlling the low-side and high-side power switches. This enables a low-power operation and a better controlled driver performance irrespective of the IC supply voltage.

Excellent delay matching of 1 ns typical is achieved for the low-side and high-side signal paths. The 4 A peak source and sink current capability of the driver's output stage guarantees short rise- and fall-times even at high loads.

The NGD4300-Q100 is offered in the HSO8 package, and operates over an extended −40 °C to +125 °C temperature range.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.



2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
  - Specified from -40 °C to +125 °C
- Input signals complying with both TTL and CMOS signaling of 2.5 V, 3.3 V, and 5 V
- Output signals with 1 ns propagation delay matching (typical)
- Propagation times of 13 ns (typical)
- Switching frequency up to 1 MHz
- 4 A peak source and 5 A sink current capability of the gate driver output stage
- 4 ns rise and 3.5 ns fall times with 1000 pF loads
- Bootstrap supply voltage up to 120 V using an integrated bootstrap diode
- 8 V to 17 V V_{DD} operation range
- Undervoltage protection for both low-side and high-side supplies
- Low-power consumption (I_{DDO}) of 0.6 mA (typical)
- 8 pin HSO8 package
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Applications

- Current-fed, push-pull converters
- Two-switch forward power converters
- Class-D audio amplifiers
- Solid-state motor drives

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NGD4300DD-Q100	-40 °C to +125 °C	HSO8	plastic thermal enhanced small outline package; 8 leads; 1.27 mm pitch; 4.9 mm × 3.9 mm × 1.7 mm body; exposed die pad	SOT8063-1

5. Marking

Table 2. Marking codes

Type number	Marking code[1]
NGD4300DD-Q100	NGD4300

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

6. Functional diagram

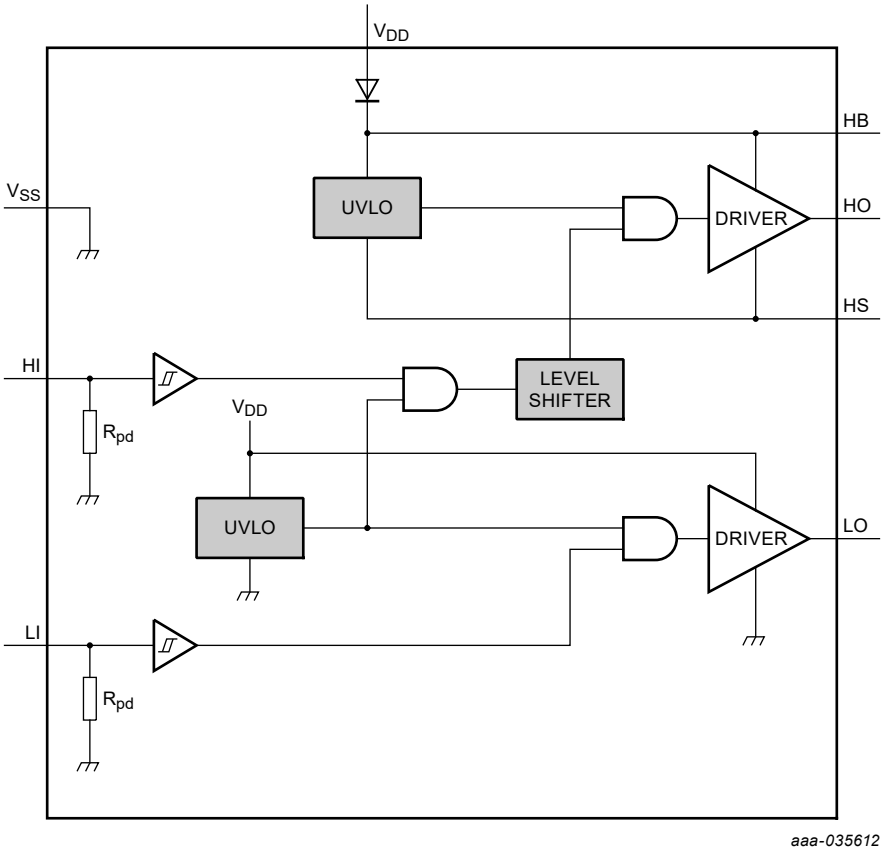
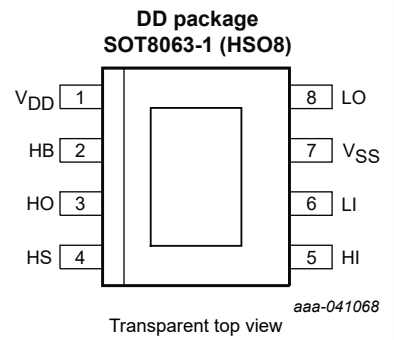


Fig. 1. Functional block diagram

7. Pinning information

7.1. Pinning



7.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
V_{DD}	1	gate drive supply voltage
HB	2	high-side gate driver supply voltage; connected to a positive terminal of the bootstrap capacitor and the cathode of the internal bootstrap diode
HO	3	driver output signal for controlling the high-side N-channel MOSFET; output is referenced to HS
HS	4	high-side source connection; reference level for the driver high-side; connected to the source of the high-side MOSFET and negative terminal of bootstrap capacitor
HI	5	high-side control input signal compatible with both TTL and CMOS signaling
LI	6	low-side control input signal compatible with both TTL and CMOS signaling
V_{SS}	7	ground (0 V)
LO	8	driver output signal for controlling the low-side N-channel MOSFET; output is referenced to V_{SS}

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to V_{SS} (ground = 0 V) unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages and currents					
V_{DD}	supply voltage on V_{DD} pin		-0.3	+20	V
V_{LI}, V_{HI}	voltage on LI or HI pins		-10	+20	V
V_{LO}	voltage on LO pin	DC	-0.3	V_{DD}+0.3	V
		repetitive pulse <100 ns	-2	V_{DD}+0.3	V
V_{HO}	voltage on HO pin	DC	V_{HS}-0.3	V_{HB}+0.3	V
		repetitive pulse <100 ns	V_{HS}-2	V_{DD}+0.3	V
V_{HS}	voltage on HS pin	DC	-5	+115	V
		repetitive pulse <100 ns [1]	-(24-V_{DD})	+115	V
V_{HB}	voltage on HB pin	referenced to V_{HS}	-0.3	+20	V
		referenced to V_{SS}	-	120	V
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-40	+150	°C
Electrostatic discharge					
V_{ESD}	electrostatic discharge voltage	HBM: ANSI/ESDA/JEDEC JS-001 class 2	-2000	+2000	V
		CDM: ANSI/ESDA/JEDEC JS-002 class C3	-1000	+1000	V

[1] Verified at bench characterization.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to V_{SS} (ground = 0 V) unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage on V_{DD} pin		8.0	-	17.0	V
V_{HS}	voltage on pin HS		-0.3	-	110.0	V
V_{HB}	voltage on pin HB		-0.3	-	110.0	V
SR_{HS}	slew rate of voltage on pin HS		-	-	50.0	V/ns
T_{amb}	ambient temperature		-40	-	+125	°C

10. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Condition	SOT8063-1	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air; JEDEC test board	38.9	°C/W
$R_{th(j-c)}$	thermal resistance from case (top) of package	in free air; JEDEC test board	29.5	°C/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	in free air; JEDEC test board	4.5	°C/W
$R_{th(j-bop)}$	thermal resistance from junction to bottom of package	in free air; JEDEC test board	13.1	°C/W

11. Electrical characteristics

Table 7. Electrical characteristics

At recommended operating conditions. Voltages are referenced to V_{SS} (ground = 0 V) unless otherwise specified.
V_{DD} = V_{HB} = 12 V; V_{SS} = V_{HS} = 0 V; no load on pins LO and HO; T_j = T_{amb}.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
Supplies (V_{DD} and HB pins)						
I_{DD}	quiescent current on pin V_{DD}	V_{LI} = V_{HI} = 0 V	0.03	0.06	0.17	mA
I_{DDO}	operating current on pin V_{DD}	f = 500 kHz	0.3	0.6	2	mA
I_{HB}	total HB quiescent current	V_{LI} = V_{HI} = 0 V	0.01	0.04	0.1	mA
I_{HBO}	total HB operating current	f = 500 kHz	0.3	0.6	2	mA
I_{HBS}	total HB to V_{SS} quiescent current	V_{HS} = V_{HB} = 115 V	0.0001	0.1	2	uA
I_{HBSO}	total HB to V_{SS} operating current	f = 500 kHz	0.001	0.05	1.2	mA
$V_{start(V_{DD})}$	start voltage on pin V_{DD}	$V_{start(V_{DD})}$ = V_{DD} - V_{SS}	6.1	7.11	7.85	V
$V_{start(hys)V_{DD}}$	start voltage hysteresis on pin V_{DD}		0.4	0.63	0.8	V
$V_{start(HB)}$	start voltage on pin HB	$V_{start(HB)}$ = V_{HB} - V_{HS}	5.8	6.5	7.5	V
$V_{start(hys)HB}$	start voltage hysteresis on pin HB		0.8	1	1.4	V
Input stage (LI and HI pins)						
V_{T-}	negative-going threshold voltage		1	1.37	1.7	V
V_{T+}	positive-going threshold voltage		1.8	2.15	2.7	V
R_{pd}	input pull-down resistance		20	68	200	kΩ
Low-side output driver (LO pin)						
$V_{OL(ls)}$	low-side low-level output voltage	I_{LO} = 100 mA, $V_{OL(ls)}$ = V_{LO} - V_{SS}	0.025	0.06	0.12	V
$V_{OH(ls)}$	low-side high-level output voltage	I_{LO} = -100 mA, $V_{OH(hs)}$ = V_{DD} - V_{LO}	0.05	0.09	0.18	V
$I_{OH(ls)}$	low-side peak pull-up current	V_{LO} = 0 V	-	4	-	A
$I_{OL(ls)}$	low-side peak pull-down current	V_{LO} = 12 V	-	5	-	A
High-side output driver (HO pin)						
$V_{OL(hs)}$	high-side low-level output voltage	I_{HO} = 100 mA, $V_{OL(hs)}$ = V_{HO} - V_{HS}	0.025	0.06	0.12	V
$V_{OH(hs)}$	high-side high-level output voltage	I_{HO} = -100 mA, $V_{OH(hs)}$ = V_{HB} - V_{HO}	0.05	0.09	0.18	V
$I_{OH(hs)}$	high-side peak pull-up current	V_{HO} = 0 V	-	4	-	A
$I_{OL(hs)}$	high-side peak pull-down current	V_{HO} = 12 V	-	5	-	A
Bootstrap diode						
V_F	bootstrap diode forward voltage	I_F = 100 µA	0.1	0.65	0.8	V
		I_F = 100 mA	0.15	0.85	1	V
$R_{dyn(bootd)}$	bootstrap diode dynamic resistance		0.3	0.5	0.85	Ω

[1] All typical values are measured at T_{amb} = 25 °C.

12. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to V_{SS} (ground = 0 V) unless otherwise specified.

For parameters definition see Fig. 2.

V_{DD} = V_{HB} = 12 V; V_{SS} = V_{HS} = 0 V; no load on pins LO and HO; T_j = T_{amb}.

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +125 °C			Unit
			Min	Typ[1]	Max	
$t_{PHL(ls)}$	low-side HIGH to LOW propagation delay	low-side turn off (LI falling to LO falling)	3	13	30	ns
$t_{PHL(hs)}$	high-side HIGH to LOW propagation delay	high-side turn off (HI falling to HO falling)	3	13	30	ns
$t_{PLH(ls)}$	low-side LOW to HIGH propagation delay	low-side turn on (LI rising to LO rising)	3	13	30	ns
$t_{PLH(hs)}$	high-side LOW to HIGH propagation delay	high-side turn on (LI rising to LO rising)	3	13	30	ns
$t_{dm(on)}$	turn-on delay matching	low-side turn on and high-side turn off	0	1	7	ns
$t_{dm(off)}$	turn-off delay matching	low-side turn off and high-side turn on	0	1	7	ns
t_r	output rise time	LO and HO outputs; C_L = 1000 pF; 10% to 90%	1.5	4	14	ns
t_f	output fall time	LO and HO outputs; C_L = 1000 pF; 90% to 10%	1.5	3.5	12	ns
$t_{pw(inp),min}$	minimum input pulse width		-	-	20	ns
$t_{off(bootd)}$	bootstrap diode turn off time	I_F = 100 mA, I_{rev} = 0.5 A	-	10	40	ns

[1] All typical values are measured at T_{amb} = 25 °C.

12.1. Waveforms and graphs

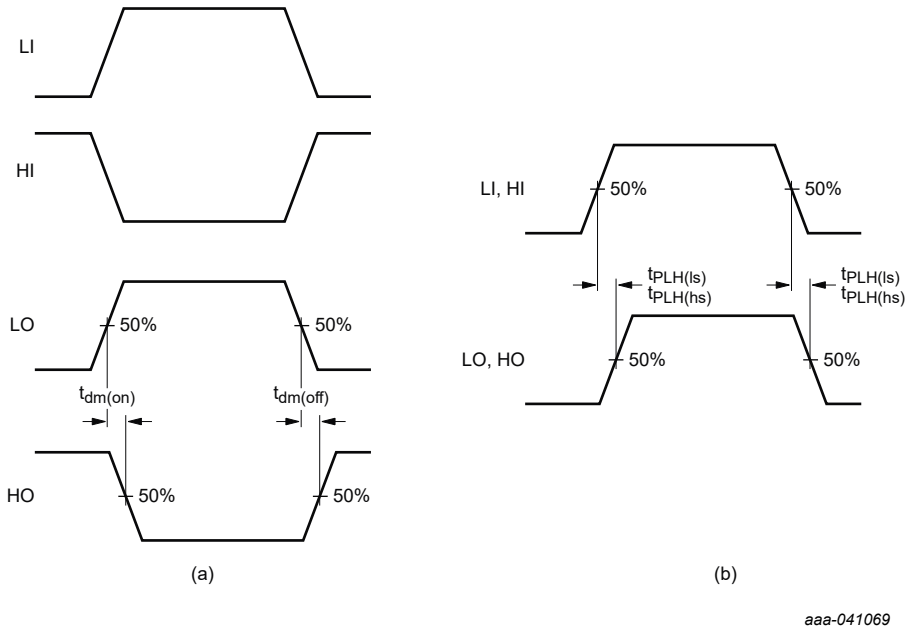
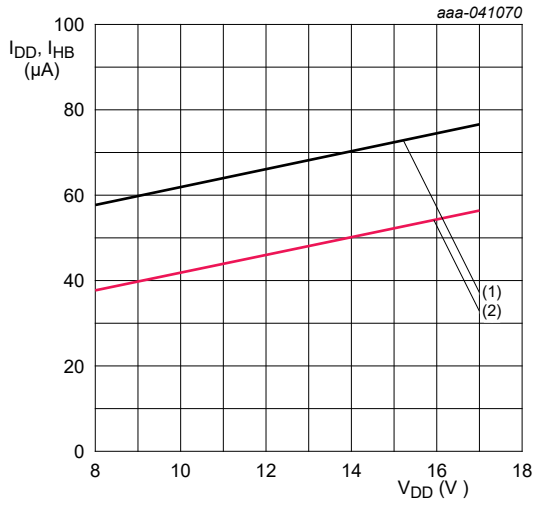
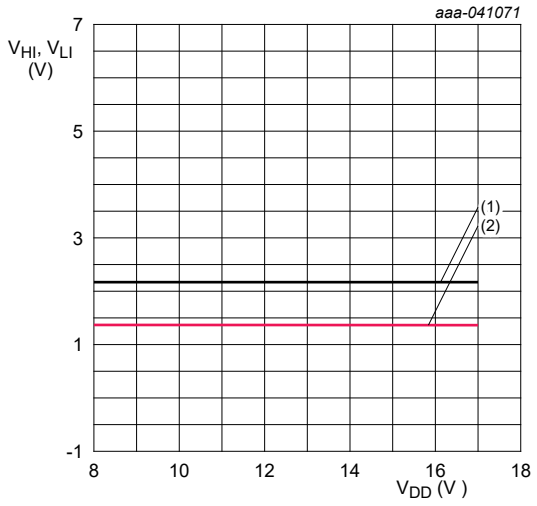


Fig. 2. The input to output delay matching (a) and propagation delays (b)



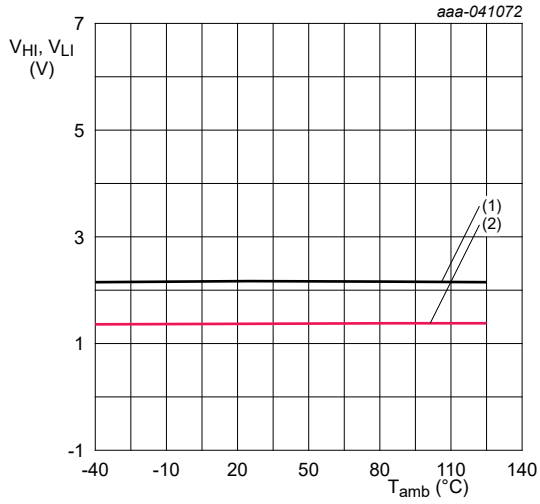
T_{amb} = 25 °C; V_{DD} = V_{HB}
(1) I_{DD}
(2) I_{HB}

Fig. 3. Quiescent current (I_{DD}, I_{HB}) versus supply voltage (V_{DD})



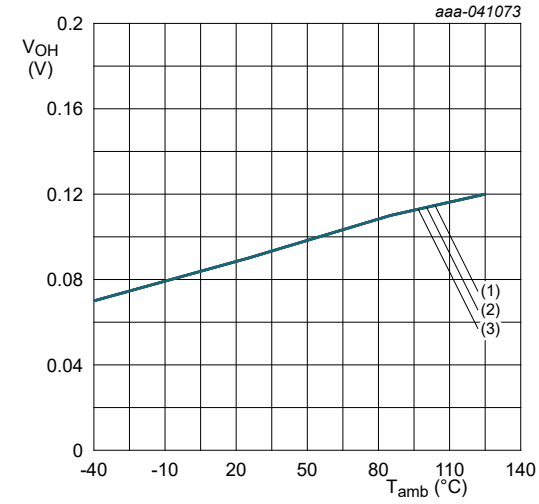
T_{amb} = 25 °C
(1) Rising
(2) Falling

Fig. 4. Input (V_{HI}, V_{LI}) threshold voltage versus supply voltage (V_{DD})



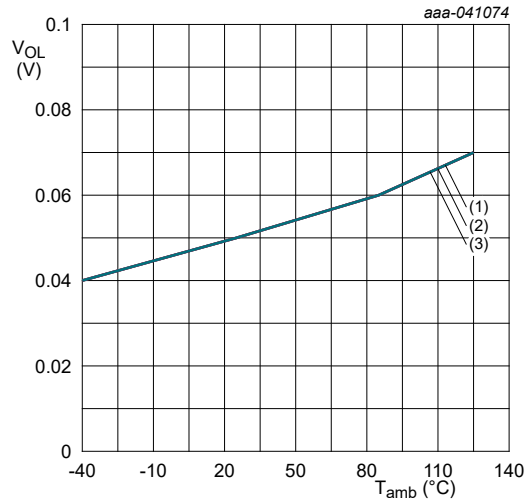
V_{DD} = 12 V
(1) Rising
(2) Falling

Fig. 5. Input (V_{HI}, V_{LI}) threshold voltage versus ambient temperature (T_{amb})



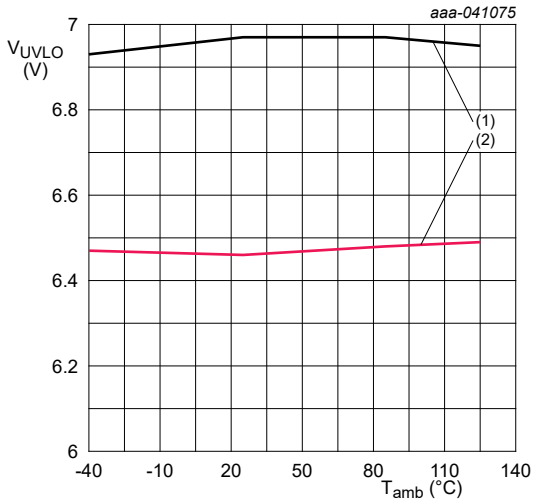
I_{HO} = I_{LO} = 100 mA
(1) V_{DD} = V_{HB} = 8 V
(2) V_{DD} = V_{HB} = 12 V
(3) V_{DD} = V_{HB} = 17 V

Fig. 6. High level output voltage ($V_{OH(LO)}$, $V_{OH(HO)}$) versus ambient temperature (T_{amb})



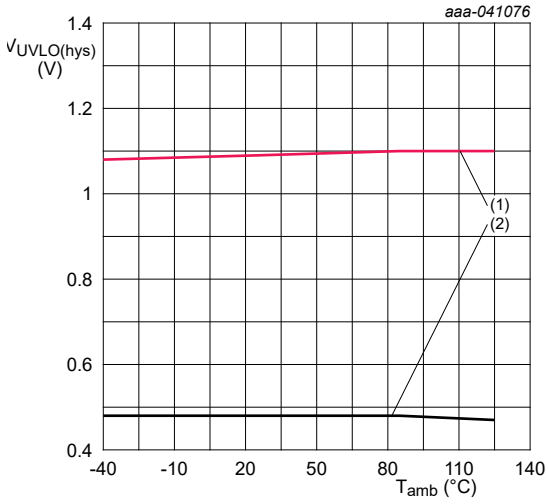
$I_{HO} = I_{LO}$ = 100 mA
(1) $V_{DD} = V_{HB}$ = 8 V
(2) $V_{DD} = V_{HB}$ = 12 V
(3) $V_{DD} = V_{HB}$ = 17 V

Fig. 7. Low level output voltage ($V_{OL(LO)}$, $V_{OL(HO)}$) versus ambient temperature (T_{amb})



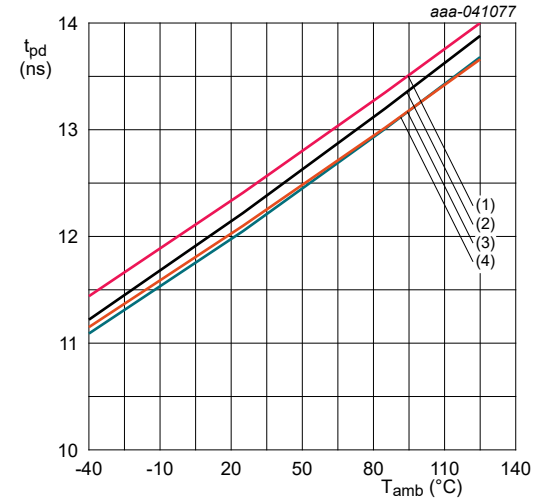
(1) V_{DD} rising
(2) V_{HB} rising

Fig. 8. Undervoltage lockout voltage (V_{UVLO}) versus ambient temperature (T_{amb})



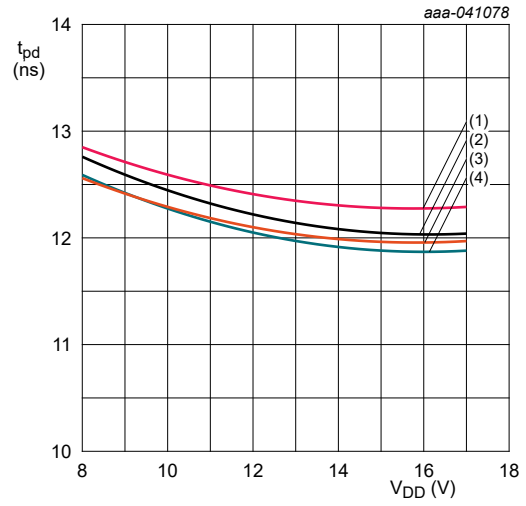
(1) V_{HB} UVLO hysteresis
(2) V_{DD} UVLO hysteresis

Fig. 9. Undervoltage lockout voltage hysteresis ($V_{UVLO(hys)}$) versus ambient temperature (T_{amb})



$V_{DD} = V_{HB}$ = 12 V
(1) $t_{PHL(ls)}$
(2) $t_{PLH(ls)}$
(3) $t_{PHL(hs)}$
(4) $t_{PLH(hs)}$

Fig. 10. Propagation delay (T_{pd}) versus ambient temperature (T_{amb})



T_{amb} = 25 °C; V_{DD} = V_{HB}

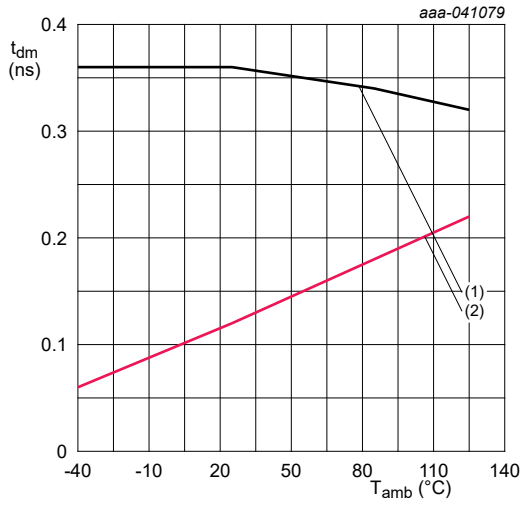
(1) $t_{PHL(ls)}$

(2) $t_{PLH(ls)}$

(3) $t_{PHL(hs)}$

(4) $t_{PLH(hs)}$

Fig. 11. Propagation delay (T_{pd}) versus supply voltage (V_{DD})

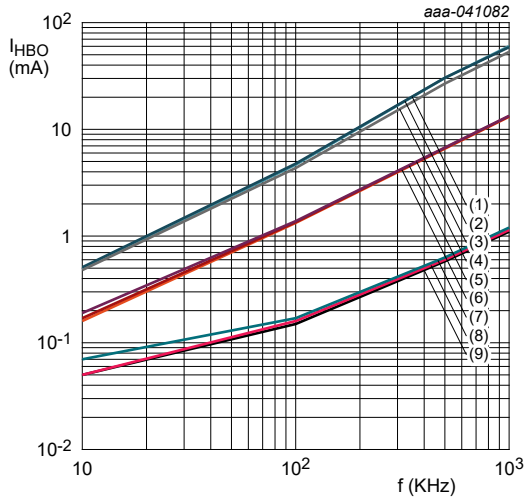


V_{DD} = V_{HB} = 12 V

(1) $t_{dm(on)}$

(2) $t_{dm(off)}$

Fig. 12. Delay matching (T_{dm}) versus ambient temperature (T_{amb})



V_{HB} - V_{HS} = 12 V

(1) C_L = 0 pF; T_{amb} = -40 °C

(2) C_L = 0 pF; T_{amb} = 25 °C

(3) C_L = 0 pF; T_{amb} = 125 °C

(4) C_L = 1 nF; T_{amb} = -40 °C

(5) C_L = 1 nF; T_{amb} = 25 °C

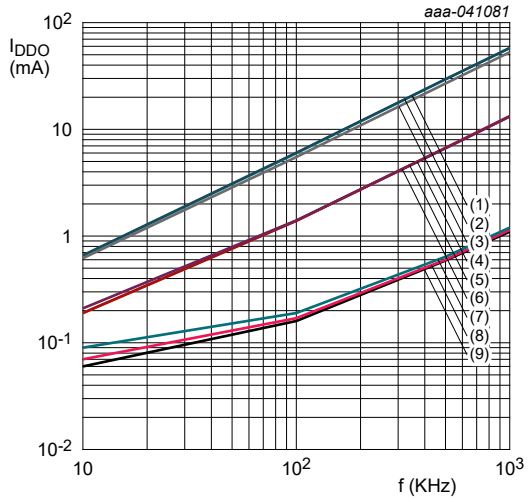
(6) C_L = 1 nF; T_{amb} = 125 °C

(7) C_L = 4.7 nF; T_{amb} = -40 °C

(8) C_L = 4.7 nF; T_{amb} = 25 °C

(9) C_L = 4.7 nF; T_{amb} = 125 °C

Fig. 13. Operating current (I_{HBO}) versus frequency



V_{DD} = 12 V

(1) C_L = 0 pF; T_{amb} = -40 °C

(2) C_L = 0 pF; T_{amb} = 25 °C

(3) C_L = 0 pF; T_{amb} = 125 °C

(4) C_L = 1 nF; T_{amb} = -40 °C

(5) C_L = 1 nF; T_{amb} = 25 °C

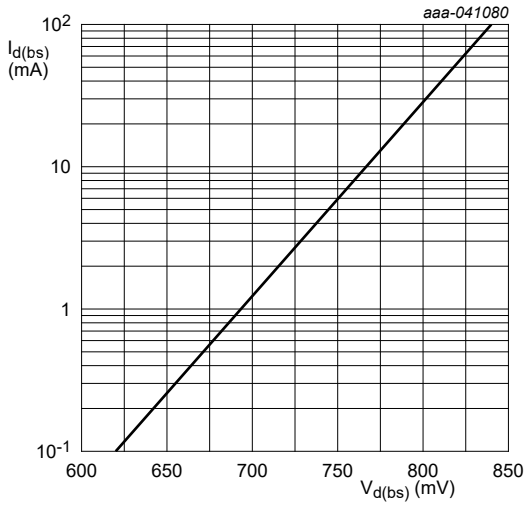
(6) C_L = 1 nF; T_{amb} = 125 °C

(7) C_L = 4.7 nF; T_{amb} = -40 °C

(8) C_L = 4.7 nF; T_{amb} = 25 °C

(9) C_L = 4.7 nF; T_{amb} = 125 °C

Fig. 14. Operating current (I_{DDO}) versus frequency



T_{amb} = 25 °C

Fig. 15. Bootstrap diode current ($I_{d(bs)}$) versus bootstrap diode voltage ($V_{d(bs)}$)

13. Detailed description

13.1. Overview

The NGD4300-Q100 is a high-performance cost-effective gate driver meant for driving both high-side and low-side N-channel MOSFETs in a synchronous buck or a half-bridge configuration. The IC can be directly connected to a low-voltage PWM controller providing TTL- or CMOS-compatible signals to control independently external power MOSFETs. The low-side and high-side signal paths up to the output stage driving external power transistor are supplied from an internal low-voltage supply. This reduces the overall power consumption and makes the propagation delay independent of the IC supply voltage V_{DD}. Excellent matching of propagation delays of low-side and high-side signal paths is guaranteed.

The NGD4300-Q100 internally generates a floating supply for a high-side MOSFET using an on-chip bootstrap diode and an external capacitor. Maximum allowed voltage on the HB pin is 120 V. The sink and source current capability of the IC output drivers, with a peak current of 4 A, results in fast turn-on and turn-off of external power MOSFETs.

The undervoltage protection circuit available for both low-side and high-side supplies ensures the reliable operation of the IC. NGD4300-Q100 show very low operation current (0.6 mA typical) and strong noise immunity for input (-10, 20 V) and HS (-5V_{DC}) pin. NGD4300-Q100 is very suitable for high power module with high frequency operation.

13.2. Block diagrams

The NGD4300-Q100 function block diagrams is shown in Fig. 16.

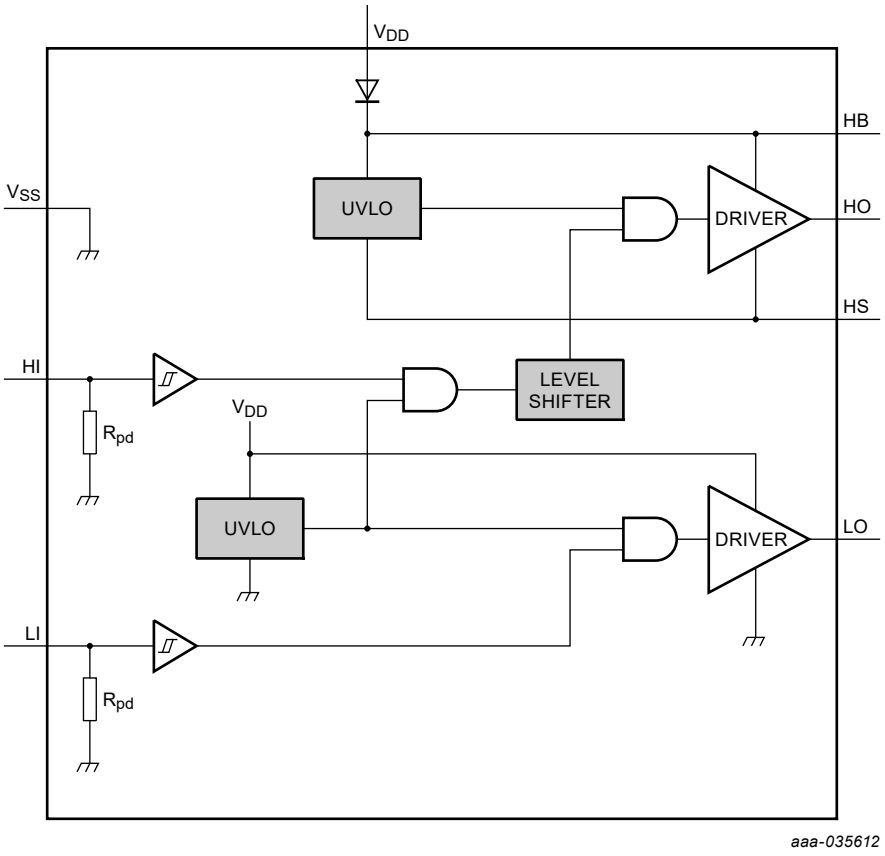


Fig. 16. Functional block diagram

13.3. Feature description

13.3.1. Undervoltage lockout (UVLO)

For the IC to work in the normal operating mode, both main supply (V_{DD} pin) and the bootstrap supply (HB-HS pin) have to be above their start levels ($V_{start(VDD)}$ and $V_{start(HB)}$, respectively). The HS and LS channels are enabled then, and the state of the IC outputs (LO and HO) depends on the state of the inputs LI and HI, respectively. The NGD4300-Q100 works as a non-inverting gate driver which means that the inputs directly influence the state of the gate driver outputs. shows the state of the outputs for different input pin state combinations. When the inputs are not driven, the internal pull-down resistors at these pins define the IC output state.

There are about 25 µs output delay during NGD4300-Q100 V_{DD} and V_{HB-HS} startup. Fig. 17show the device startup behavior. shows the device startup behavior

Table 9. Truth table

Truth table describing the NGD4300 outputs for different input state combinations in the IC operating mode.

HI	LI	HO	LO
L	L	L	L
L	H	L	H
H	L	H	L
H	H	H	H
floating	floating	L	L

Table 10.

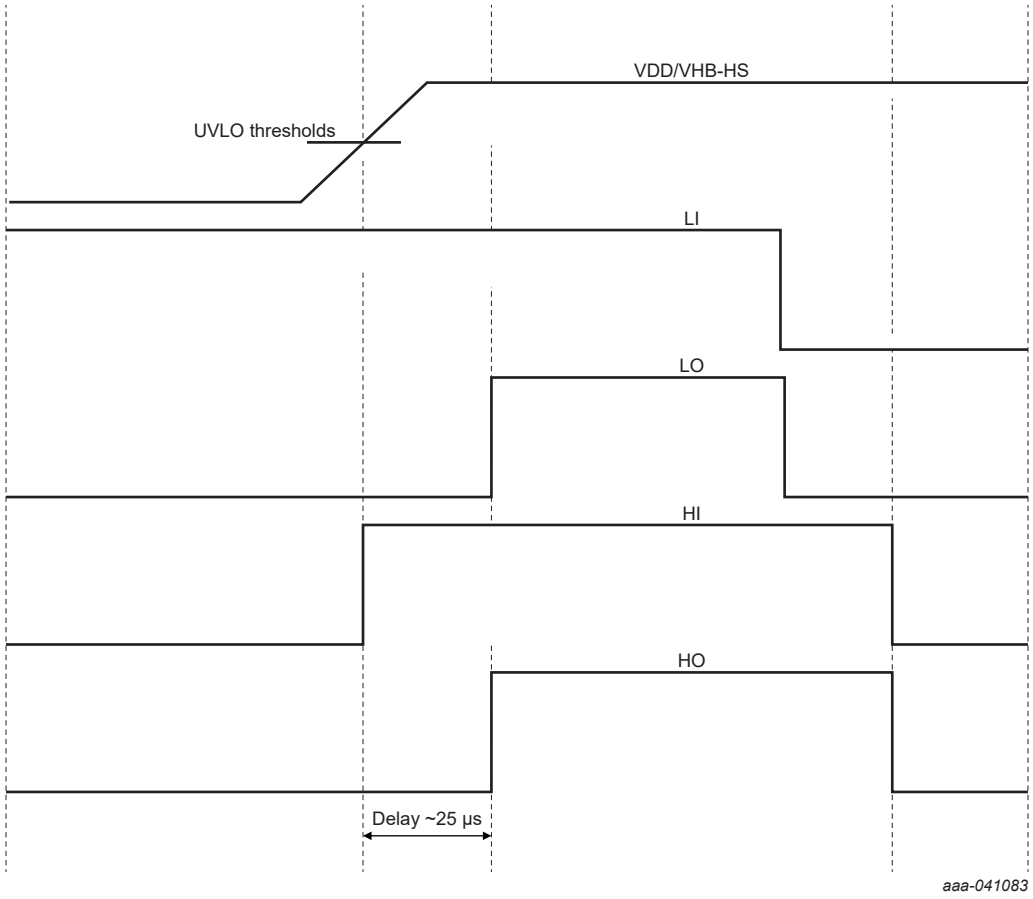


Fig. 17. Undervoltage lockout (UVLO)

13.3.2. Input stages

The input stage of the NGD4300-Q100 is COMS and TTL compatible. The logic rising threshold level is 2.2 V and the logic falling is 1.35 V. The input pin of NGD4300-Q100 can withstand voltage from -10 V to 20 V and build in hysteresis for robust noise immunity.

13.3.3. Output stages

The low-side and high-side output are independently controlled by HI and LI pin. NGD4300-Q100 provide 4 A peak source current and -5 A peak sink current for both low-side and high-side output when V_{DD} at 12 V. NGD4300-Q100 high-side and low-side output provide about 4 A output peak current even the V_{DD} voltage drop to 8 V.

13.3.4. Timing

The NGD4300-Q100 LO and HO pin both can drive a 1 nF cap load with 4 ns rise and 3.5 ns fall times. The high-side and low-side channel output delay matching achieve 1ns. The device showing very good timing performance in switching performance. Thanks to NGD4300-Q100 fast timing performance, it can help to reduce system switching loss and shorter the deadtime setting to achieve higher power system efficiency.

14. Application information

In power applications gate drivers are used to interface between PWM controllers and power switches such as power MOSFETs. A typical PWM controller has low-power CMOS outputs that are not capable of supplying the current necessary to charge/discharge the relatively high input capacitance of power switches. PWM controllers do not include level shifting to generate the voltage levels required to drive high-side power switches.

The gate driver implements level shifting between the signal levels of the PWM controller and the gate voltages required by power MOSFETs. This is especially required in high-power applications using digital controllers, where low-voltage PWM signaling (typically 3.3 V) is used to drive power MOSFETs working with gate-source (V_{GS}) voltages as high 8 V to 20 V. The use of a dedicated gate driver in such cases not only boosts the PWM signals to the required gate-drive levels, including the generation of floating supplies if needed, but also reduces conduction losses. The integration of a bootstrap diode in the NGD4300 as part of the floating supply reduces the number of external components.

Gate drivers such as the NGD4300-Q100 combine a high-impedance low capacitance input stage with high output-current drive. The high-impedance low capacitance input stage can be driven at high frequency by a PWM controller. The high current capability of the output driver in the NGD4300-Q100 allows rapid charge and discharge of power switch capacitances and consequently faster power switching at reduced power losses. Power conversion at higher switching frequencies is especially advantageous in DC/DC converters. It enables the use of smaller-value capacitors and inductors in the converter circuit, and this means a much smaller footprint of the overall power solution.

Gate drivers also shield the power stage from switching noise and thermal stress. This improves the power efficiency and reliability of the application.

The NGD4300-Q100 gate driver switches two N-channel power MOSFETs, one high- side and one low-side.The power MOSFETs can be configured in half-bridge, full-bridge or synchronous buck converter topologies. Both power MOSFETs are controlled by independent input signals (LI and HI),which offers full flexibility in setting their on- and off-times. Since the NGD4300-Q100 inputs can be driven by low-voltage domain signals, the switching losses of the gate driver can be reduced. The output signals driving the high-side power MOSFET are level-shifted using a floating supply that comprises an integrated boost diode and an external boost capacitor. The maximum input voltage of the power stage, which is connected to the drain voltage of the external high-side N-channel MOSFET, is 120 V.

14.1. Typical application circuit

Fig. 18 shows a typical application of the NGD4300-Q100 driving power MOSFETs in a synchronous DC/DC buck converter. Unlike common gate drivers with similar functionality, the NGD4300-Q100 can be connected directly to a low-voltage PWM controller, such as the 3.3 V controller shown in the figure. The low-voltage PWM controller and the NGD4300-Q100 internally generated low-voltage supply reduce the power dissipation of the application. Only the output drivers of the NGD4300-Q100 are supplied directly from the V_{DD} supply. To ensure a stable supply, a bypass capacitor is required between V_{DD} and V_{SS} pins. The input voltage (V_{IN}) of the buck converter in the figure is 120 V.

Bootstrap resistor (R_{boot}) in series with the bootstrap capacitor (C_{boot}) reduces the inrush current through the integrated bootstrap diode during the gate driver high-side supply start-up. This resistor also limits the ramp up slew rate of the high-side voltage (V_{HS} - V_{HS}). Additional resistors (R_{gate}) can be placed between the outputs (LO, HO) and the gates of the power MOSFETs to adjust the power MOSFETs' switching times. They also help to reduce ringing caused by parasitic inductance in the system and to adjust the dynamic power losses in the IC itself. In applications requiring very fast turn-off times, anti-parallel diodes (not shown) can be placed in parallel with the gate resistors. These diodes will bypass the gate resistors during turn-off and reduce the turn-off transition time.

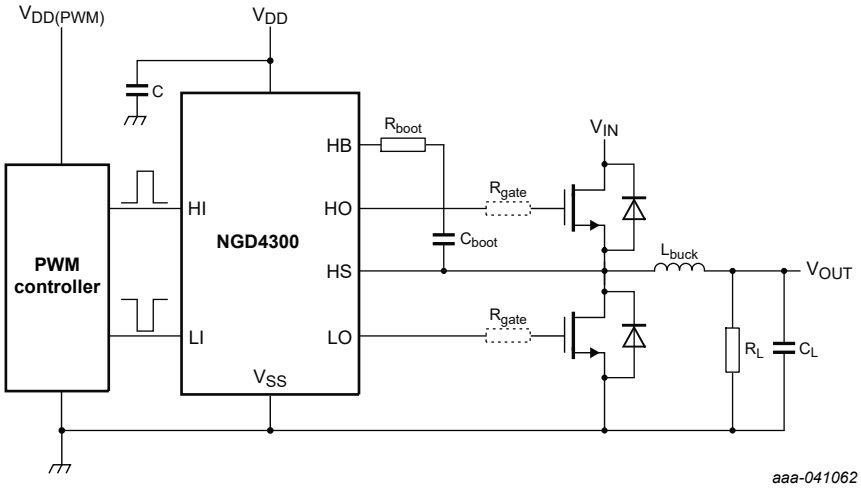


Fig. 18. NGD4300-Q100 driving power switches in a synchronous buck converter

14.2. Application curves

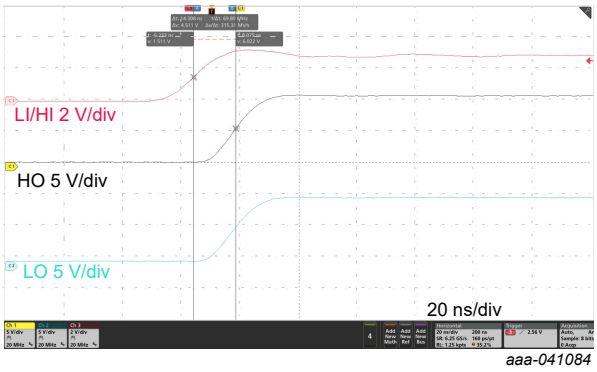


Fig. 19. Turn-on propagation delay

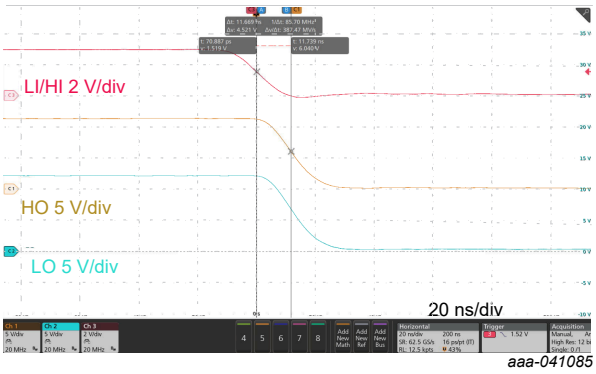


Fig. 20. Turn-off propagation delay

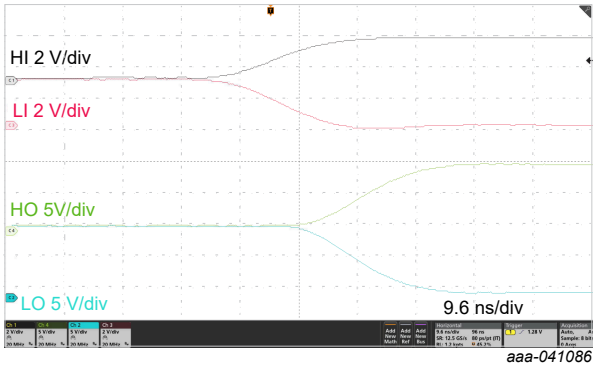


Fig. 21. Delay matching

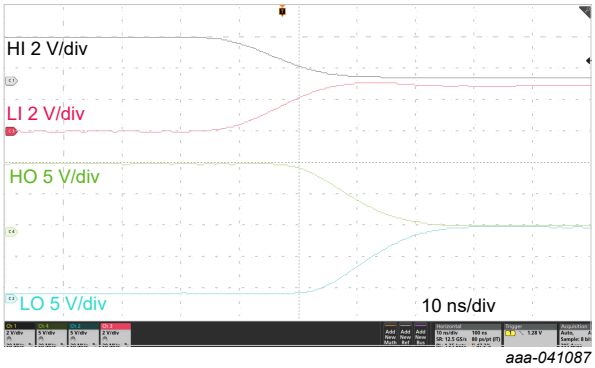


Fig. 22. Delay matching

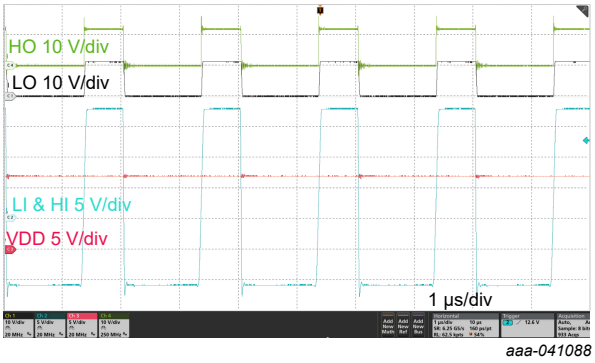


Fig. 23. Input side maximum rating

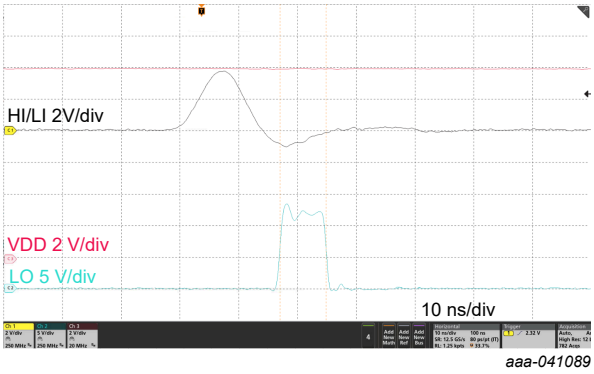


Fig. 24. Minimum turn-on time

15. Power supply recommendations

The NGD4300-Q100 works with the main and bootstrap supplies, both requiring proper decoupling/filter capacitors.

For the main supply, a decoupling capacitor needs to be placed between the V_{DD} and V_{SS} pins of the IC, preferably as close to those pins as possible. A low-ESR, ceramic surface mount capacitor is recommended. For more optimized performance, Nexperia recommends the use of two capacitors at this supply:

- 100 nF, ceramic surface-mount capacitor for high-frequency filtering
- 220 nF to 10 µF, for IC bias requirements

The NGD4300-Q100 bootstrap supply provides the current pulses to the high-side (HO) output pin. Therefore, similarly to the main supply, a smaller 22 nF to 220 nF local decoupling capacitor is recommended between the HB and HS pins on the IC.

16. Layout guidelines

The NGD4300-Q100, as any typical gate driver IC, will experience high di/dt during the switching transitions. Therefore any parasitic inductance in the system should be minimized to avoid excessive ringing and undesired voltage drop. PCB traces should be kept as short and wide (>20 mil) as practical. The input and bootstrap capacitors should be placed as close as possible to the IC pins. The current loops in the PCB design should be minimized. The V_{SS} pin of the NGD4300-Q100 should be placed as close as possible to the source of the low-side MOSFET. The number of vias should be maximized to ease the thermal conduction away from the driver.

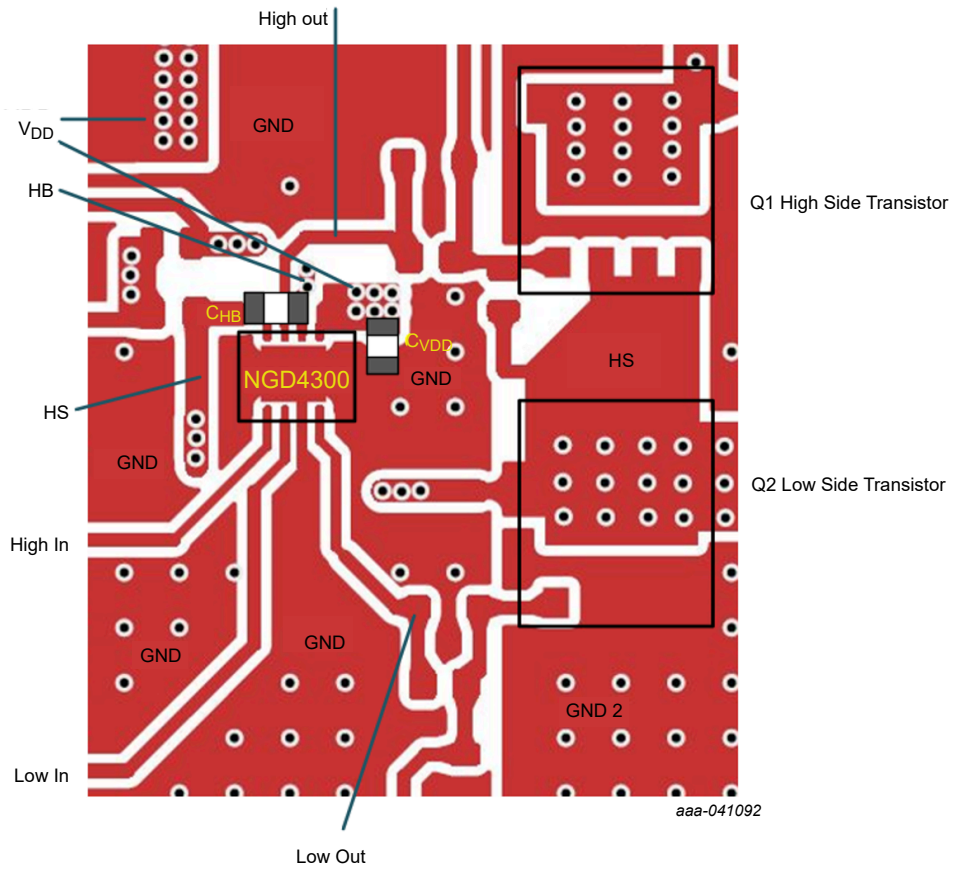
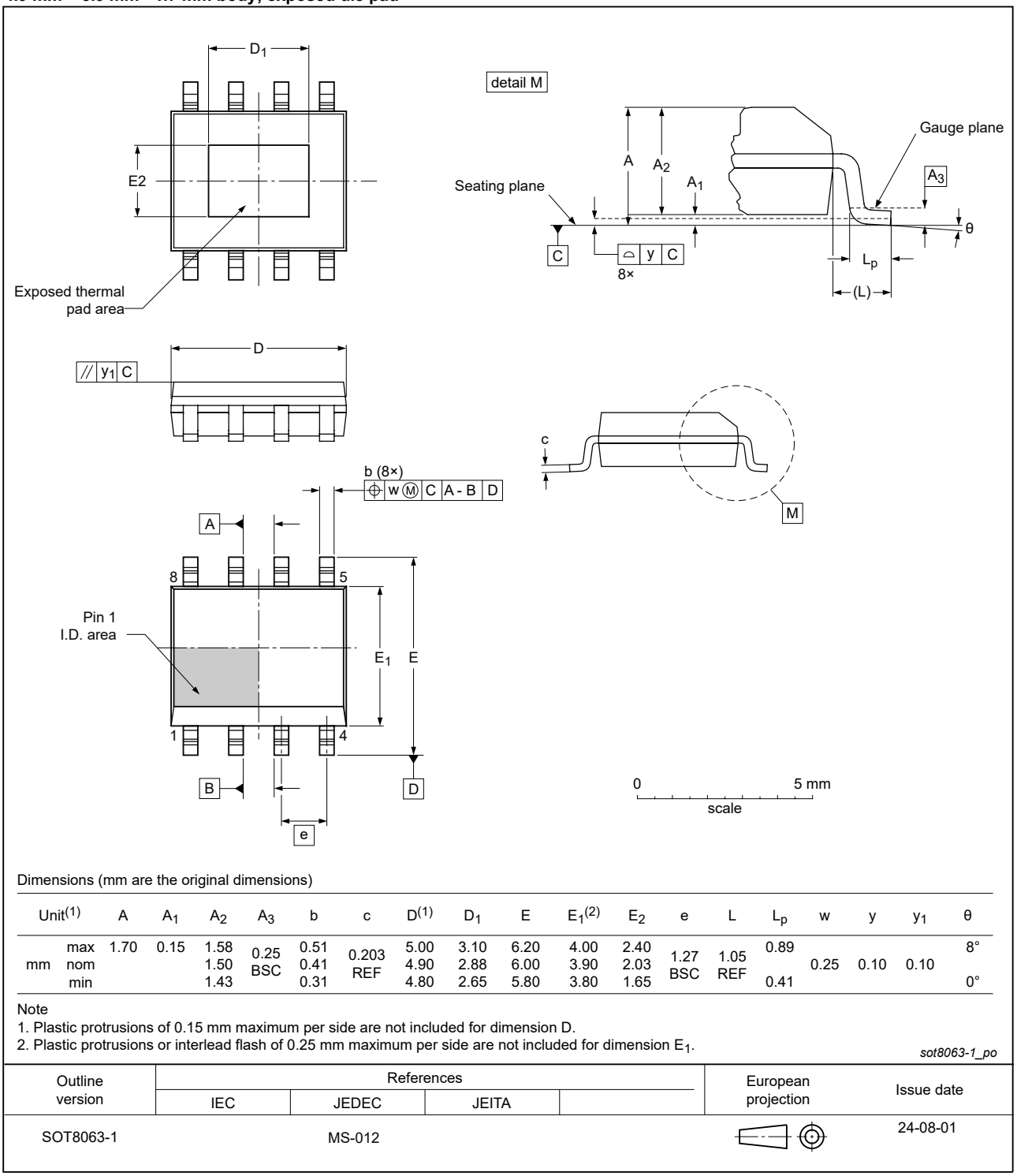


Fig. 25.

17. Package outline

HSO8: plastic thermal enhanced small outline package; 8 leads; 1.27 mm pitch; 4.9 mm × 3.9 mm ×1.7 mm body; exposed die pad

SOT8063-1



Dimensions (mm are the original dimensions)

Unit[1]		A	A_1	A_2	A_3	b	c	D[1]	D_1	E	E_1[2]	E_2	e	L	L_p	w	y	y_1	θ
mm	max	1.70	0.15	1.58	0.25	0.51	0.203	5.00	3.10	6.20	4.00	2.40	1.27	1.05	0.89	0.25	0.10	0.10	8°
	nom			1.50	BSC	0.41	REF	4.90	2.88	6.00	3.90	2.03	BSC	REF					
	min			1.43		0.31		4.80	2.65	5.80	3.80	1.65			0.41				0°

Note
1. Plastic protrusions of 0.15 mm maximum per side are not included for dimension D.
2. Plastic protrusions or interlead flash of 0.25 mm maximum per side are not included for dimension E_1.

sot8063-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8063-1		MS-012				24-08-01

Fig. 26. Package outline SOT8063-1 (HSO8)

18. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
IC	Integrated Circuit
JEDEC	Joint Electron Device Engineering Council
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
TTL	Transistor-Transistor Logic
UVLO	UnderVoltage LockOut

19. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NGD4300_Q100 v.2.1	20250718	Product data sheet	-	NGD4300_Q100 v.2
Modifications:	• Table 7: The typical values of low-side and high-side peak pull-down current updated.			
NGD4300_Q100 v.2	20241111	Product data sheet	-	NGD4300_Q100 v.1
Modifications:	• Section 14.2: Figure titles added for better readability and Fig. 20 corrected (errata).			
NGD4300_Q100 v.1	20240927	Product data sheet	-	-

20. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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